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Investigation on Thermal Resistance of Cracked AlInGaP Die Substrate and In-line Die Crack Testing Method

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Abstract

This paper has demonstrated correlation between cracks at an LED germanium (Ge) substrate to its thermal resistance. The finding shows, the R_{th} value, increases with the crack severity. Further analysis, shows the presence of many cracks inside the Ge-substrate, that were die attach at bond-force 140 gF as compared to at 60 gF. This impedes the heat flow and thus cause increase in R_{th} value. A unique test apparatus that uses Temperature Sensitive Parameters (TSP) method was designed to capture the voltage variation of cracked-dice. The results proofed, this apparatus successfully detects cracked-dice without compromising the testing throughput time.

Keywords: Crack die; Germanium substrate; Thermal resistant; Crack detection; Testing technology

Introduction

It is common to see LED in our daily life- streets lights, homes, automotive, electronic appliances and many more applications have adopted this efficient lighting product. However, as the need for brighter LED increases [1], the LED thermal management is becoming more and more important to achieve good reliability and optimal performance of LED [2]. However, the ability to prevent LEDs from overheating is the most challenging task for thermal designers. A proper cooling method plays an important role in the success of LEDs [3]. The temperature elevation of the junctions drives the need for thermal characterization of LED packages since higher junction temperatures are associated with reduced operation life [4-6].

Cracked die in LED industry is always a major concern. It causes LED reliability issues and, to a certain extent, LED failures. Periodical on-off switching and variation of environmental temperature during LED operation will induce cyclic stress on the LED. As stress increases in cyclic mode, the crack will start to form and lead to fatigue failure [7,8]. This directly affects the LED reliability. Isolating these cracks has become a challenge. Especially cracks at the bottom of the die because it is hidden; back of the die will be attached with glue to a substrate. In view of this situation, this research was carried out to investigate the correlation of this crack to thermal resistance (R_{th}) and find a plausible testing method to isolate the unit with and without cracks. The LED and substrate investigated was Aluminium Indium Gallium Phosphate (AlInGaP) and Germanium (Ge) respectively.

Theoretical Background

LED thermal resistance

In a packaged LED, its temperature rise has strong dependence on the thermal properties of the thermal path, such as chip, solder, adhesive and package. The LED consists of a chip mounted on a lead frame by solder or bonding adhesive as illustrated in Figure 1. The leads consist of high-conductivity material such as copper. The primary thermal path of the heat flow is from the junction through the lead frame to the end of the leads by heat conduction. This thermal path can be illustrated in an equivalent circuit diagram as shown in Figure 2. The thermal resistance of the LED, R_{thJS} is the sum of the thermal resistance in the LED as illustrated in the green box in Figure 2.

Thermal resistance of the LED is calculated using equation 1 [9,10]:

$$R_{thJS}=(Tj - T_s)/P_h \quad (1)$$

Tj is the junction temperature, T_s is the solderpoint temperature, usually the delta, $\Delta T=Tj - T_s$ is called temperature rise. P_h is the supplied power which dissipates in the form of heat. From equation 1, we can define the real thermal resistant, R_{th} as:

$$R_{th=}\Delta T/P_h$$
$$=\Delta T/(P_{el} - P_{opt}) \quad (2)$$

Where P_h is heating power, P_{el} is electrical power and P_{opt} is the optical power of the LED [10].

The thermal resistance of an LED can also be measured. In this paper, we used the temperature sensitive parameter (TSP) method. This is done in accordance with the JEDEC JSD51-1 standard. It uses fast-

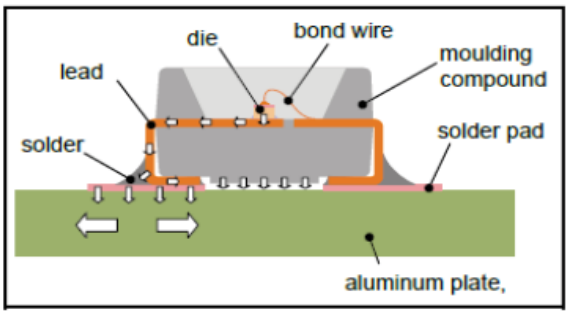

Figure 1: Internal Structure of a Surface Mount Technology in an LED Package [9].

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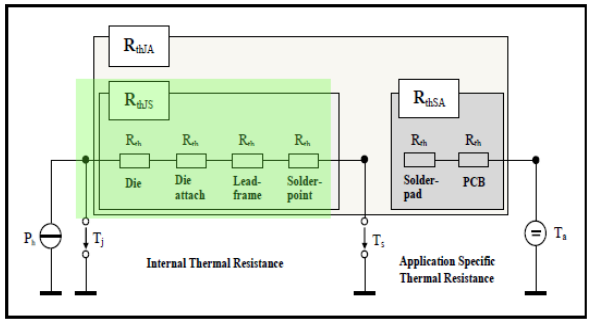
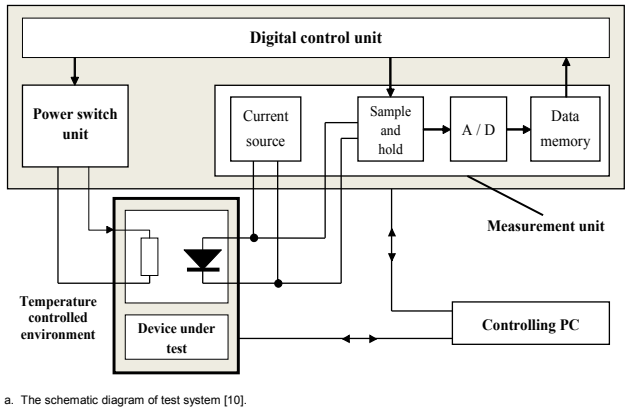
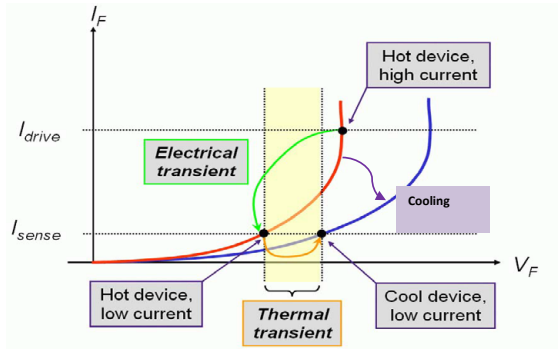


Figure 2: Static equivalent circuit.



a. The schematic diagram of test system [10].



b. Transient processes due to switching , shown in the I- V diagram

Figure 3: Schematic of the thermal transient measurement of an LED device in a combined arrangement.

switch techniques to measure the temperature rise (ΔT) immediately after removal of operational (high) current of LEDs as illustrated in Figure 3a. As soon as the high current is supplied to LEDs, the power could cause the temperature of active region to rise up. A sensing (low) current will be supplied to measure the voltage at hot and cold device to obtain voltage change, ΔV. As long as the voltage difference ΔV at testing current is caused by the supplied power, ΔT can be obtained from the linear relation [9] as described by equation 3.

$$\Delta T=\Delta V/\alpha. \quad (3)$$

α is temperature coefficient, defined as the slope of changes in T_j and forward voltage, V_f as illustrated in Figure 3b. The recorded curve of ΔT with the time is called heating response curve is illustrated in Figure 4. It records from several microseconds at the beginning up to several hundred seconds at the steady state. This curve can be further analysed and transposed to cumulative structure functions and differential structure functions curve.

R_{th} Measurement techniques

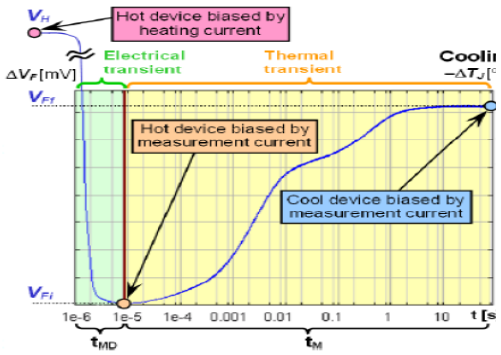
In a normal operating LED, the self-heating effect of a large working current could affect the linear relationship of forward voltage with temperature. Therefore, an accurate small current which doesn't produce thermal dissipation is applied in testing the forward voltage difference [ΔV]. Thus, the high current state and low current state must be separated and the testing accuracy depends on the transition speed between the two states. A computer controlled microsecond level switch circuit as illustrated in Figure 3c, was designed to achieve the fast transition. It is able to switch the device under test (DUT) from the driving (high current) state to the sensing (low current) state (under 5 mA accurate current) within 5 microseconds [10]. A 12-bit high speed A/D converter is adopted to achieve the data acquisition. The response of both states is illustrated in Figure 3a where high current curve and low current curve plotted shows the electrical and thermal transient. For this investigation, the LED is operated at a high current level (100 mA). This high current heat up the junction and therefore the initial thermal steady-state in this case is the hot state of the junction. Then, switching is done within 5 μs from the high (heating) current to low (sensing) current (5 mA) for the actual thermal measurement.

Material and Method

The experiment methodology is described in the process flow as shown in Figure 5.

Samples preparation

Several AlInGaP dies with size of 300 μm width by 300 μm length and with thickness of 190 μm were selected for this experiment. They were serialized in a mylar for traceability purposes. Die attach equipment was used to create cracks at die substrate because it



Source: Jedec 51-51

Figure 4: Electrical and therrmal state transitions of an LED shown as a time diagram after time distance.

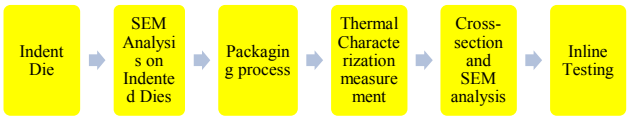


Figure 5: Showing the experiment procedure.

represent the actual situation of stress the die experiences. Cracks usually occur during the die eject and pick-up process on illustrated in Figure 6. The die attaches process follows in sequence. The die on the mylar is positioned on top of ejector pin. The ejector pin pushes the die. The bond head on the other hand comes down to pick the die. The bond head touches the die; the ejector pin continues to push the die upwards until it reaches certain height where the die will be totally released from the mylar. Bond heads pick up the die and place it to the package or lead frame. This process continues. The maximum stress the die endures is when the ejector pin pushes the die directly hitting the bond head as illustrated in the box at Figure 6.

Die Attach (DA) equipment was set up. The ejector pin and bond head were checked for the alignment and bonding stability. Keyence bond force tester was installed on the bonder to check the force. Several bonding trials were carried out to check the bonding consistency. Final confirmation of the bonding consistency was carried out by using a hand held force tester - the Correx Tension Gauge [11-13]. This is to counter confirm the Keyence bond force tester measurement accuracy before commencing the experiment. The experiment commenced with indenting 60 gF and continued with 100 gF, and 140 gF.

Crack analysis and thermal resistance measurement

The indented dies were analysed using Scanning Electron Microscope (SEM) for the crack formation. Some of the indented dies were packaged on a stable LED package and underwent electro-optical test. Each cell, several units that passed the electro-optical test, were selected for thermal characterization using T3ster in accordance to Jedec standard JESD51-51 [14].

The DUT is on a plate with a controllable temperature unit. A semiconductor cooler is used as the heat and cool source with a dual direction temperature control. Firstly, the plate temperature was set and the forward voltages tested under small testing current, then the platform temperature was changed. The test was repeated under different temperatures so that the temperature coefficient α can be obtained by linear fitting method. The operation current, various time parameters and the testing sequences were set by a PC program.

The testing began with editing a testing sequence including operation current and its applied time from 10 μs up to 100 s by linear steps on a logarithmic time axis. The temperature platform is set to a temperature T_o and the testing starts. The ending time of each operation current stimulates the program sending an instruction to A/D to test the forward voltage difference within 5 μs. The time interval between two tests, defined as the recovery time, was long enough for the DUT to recover to thermal equilibrium with the environment completely so that the temperatures of DUT for each current pulse have the same starting point. Then, next test would be performed. Actually, such a testing sequence simulates the real temperature rise process. The thermal impedance chart was plotted to see the correlation between cracked die with different bond forces against the thermal resistance values. Some of the LEDs from each bond force cells were mechanically cross-sectioned and analysed using SEM for crack propagation and gaps in the cracks. This is to correlate the thermal resistance value against the cracks and bond force induced on these dies.

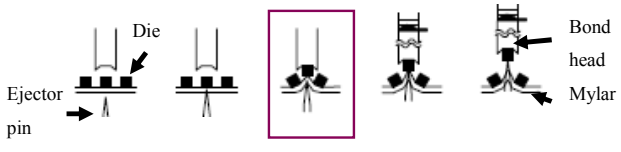


Figure 6: Die bonding sequence diagram showing ejector pin and bond head picking up the die [12].

Inline thermal transient testing (ΔV_f sequence test)

The inline testing apparatus was specially designed to detect the thermal transient of the LED at high speed. It was incorporated on the test equipment to isolate units with and without cracks. In Figure 7a and 7b shows the test equipment and the ΔV_f sequence test module. The test equipment requires two Keithley Source Measurement Unit (SMU) equipment to enable to switch between drive current, I_d and sensing current, I_s within a few micro-seconds and measure the voltage of hot device and cold device at low current. The voltage change is in micro-volts and these SMU has the capability to measure them. The voltage change is described by equation 4:

$$\Delta V_f = V_{f2} - V_{f1} \quad (4)$$

V_{f2} is voltage of cool device biased by sensing current and V_{f1} is voltage of hot device biased by sensing current as illustrated in Figure 3a and Figure 4.

The ΔV_f sequence test follows as below:

a. Binning tests at 100 mA, ~25 ms (heating phase)

b. V_{f1} at I_f=5 mA, t_p=5 μs, V_f measurement after 0.9 ms, integration 0.2 ms (1st measurement, heating phase)

c. V_{f2} at I_f=5 mA, t_p=5 μs, V_f measurement after 0.9 ms, integration 0.2 ms (2nd measurement).

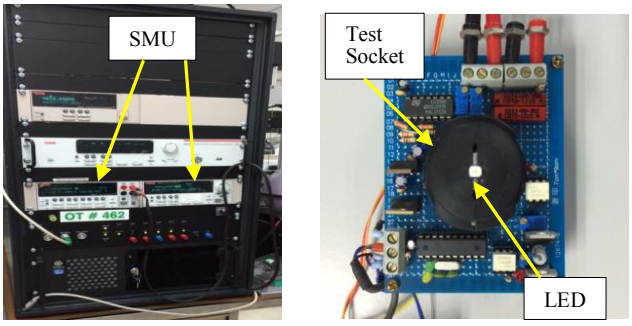
d. $\Delta V_f = V_{f2} - V_{f1.}$

The test sequence was encoded into a test program before testing was initiated. The testing equipment was calibrated using with and without cracked die units, in which the crack severity had been analysed earlier. These units are the reference units. In the set up stage, units with 60 gF (without crack) passed the test and units from 100 gF and 140 gF which have cracks failed the test. Upon completion of the set-up a total of 300 units with and without cracks were tested. The results will be further elaborated in next chapter.

Results and Discussion

Crack formation against bond force

The crack formation after indented with various bond force shows that the Ge substrate of AlInGaP dies were cracked at surface level with different crack severities.



a. Tester with Source meter. b. ΔV_f sequence test module, with LED on the test socket.

Figure 7: Testing equipment used for testing the cracked die.

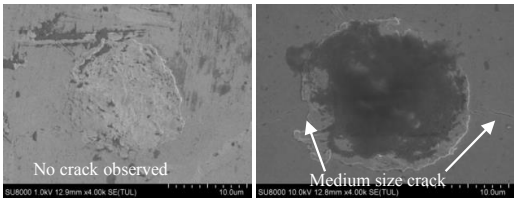
Figure 8a-8c show cells with dies bonded at 60 gF, 100 gF and 140 gF. At 60 gF, no crack is observed. However, at 100 gF and 140 gF cracks were observed. As the bond force increases, the crack severity gets worse. This is due to large amount of dislocation generation in this specimen as a result of the increasing bond force that breaks the inter-atomic bond. This crack phenomenon is in line with the Griffith energy balance criterion [15]. In this concept, all the potential energy released was used in the creation of new free surface on the crack faces [16].

As the force increases, the energy exerted to the Ge atomic bond also increases proportionally and more bonds were broken which results in increase of crack length. The findings from this evaluation shows the bond force directly influence the crack formation at the Ge substrate. The higher the bond force asserted on the die substrate through ejector pin, the more severe the crack formed [17].

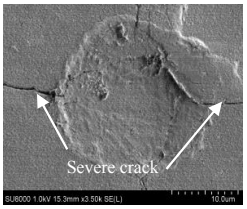
Correlation between cracked die and the die thermal resistance

Several units were taken from each cell (that were indented with various bond force) and had their thermal characteristic characterized. The temperature rise was plotted as illustrated in Figure 9a. The curve clearly shows units with high bond force (140 gF) that have larger cracks have high temperature rise compared to units with a lower bond force (60 gF) that have no cracks. A clear separation of temperature curves among these bonded units can be seen within the zone of several miliseconds in the temperature rise curve in Figure 9a.

Both cumulative structure functions curve and differential structure functions curve as illustrated in Figure 9b and c clearly show different R_{th} value of the chips bonded with different bond forces. The dies bonded with 140 gF have high R_{th} value compare to dies bonded with 100 gF and 60 gF respectively. The differences of thermal resistance between dies bonded at 60 gF and 140 gF is 35 K/W. On the other hand thermal resistance difference between 100 gF and 140 gF is 20 K/W. That shows the thermal resistance increases as the crack severity increases, this is as a result of high bond force asserted on the die substrate. To further understand this correlation, units bonded at 60 gF and 140 gF were mechanically cross sectioned and SEM analysis was carried out. The cross sections are as illustrated in Figure 10a and 10b. The conductive silver filled glue bond line thickness between both cells, at 60 gF and 140 gF are almost the same. This means the impact of silver filled glue to the thermal conductivity are the same for both cells.

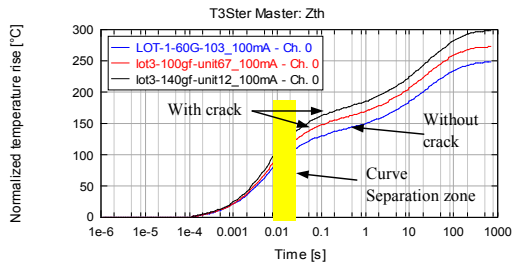


a. 60gF bond force b. 100gF bond force

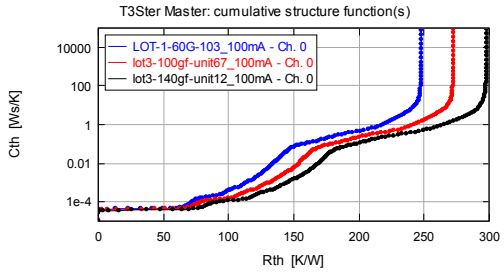


c. 140gF bond force

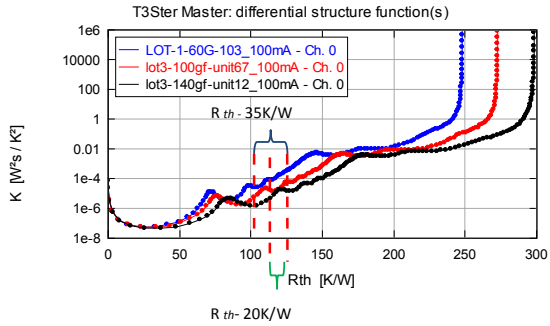
Figure 8: SEM photo shows the images of dies indented with different bond forces.



a. Normalized temperature rise curve of cracked LED with different die attach bond force.



b. Cumulative structure functions of cracked LED with different die attach bond force.



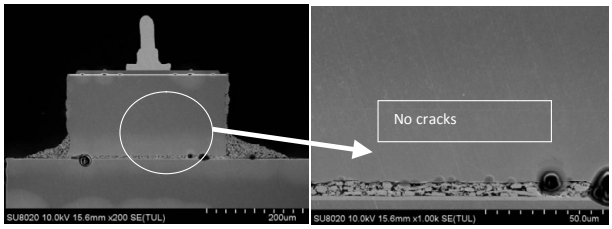
c. Measured differential structure functions of cracked LED with diffent die bond force.

Figure 9: Cracked LED measured for Thermal Resistance on T3ster.

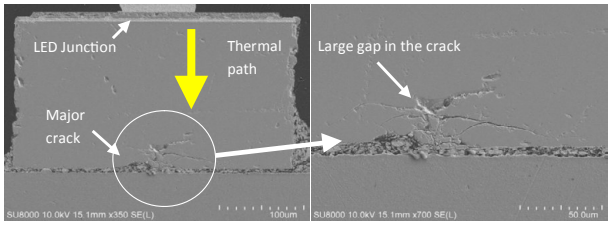
Hence, it won't influence the R_{th} difference between 60 gF and 140 gF indented units.

Die bonded at 60 gF as illustrated in Figure 10a shows no cracks. Hence, there's lesser impedance to heat flows in the Ge substrate during the LED operation. On the other hand, those dies bonded at 140 gF as illustrated in Figure 10b show large cracks inside the Ge substrate. Such cracks create gaps that prevent good flow of heat from the LED junction which increases the thermal resistance value. This finding is quite similar to work done by M. Rancz et al. [18]. In this work, they evaluated units with and without voids at Thermal Interface Material (TIM) in between chips and packages. Their finding shows R*th* value in units with large voids is higher compare to no void. They conclude the large voids or gaps within the units impede the heat flow. The bigger the gap that impedes the thermal flow, the bigger the R_{th} value. This finding is quite similar to our finding on cracked die in LED.

The gaps caused by cracks is usually filled with air and it is known to have poor thermal conductivity, K. Hence when the thermal conductivity drops, R_{th} increases as described in equation 5 [19,20].



a. Cross section view of 60gF bond force unit. Small gaps were observed inside the Ge substrate.



b. Cross-section view of 140gF bond force. Big gaps along the crack lines.

Figure 10: Shows the SEM photo of cross-sectioned die at 60gF and 140gF.

$$R_{th}=t/K.A \quad (5)$$

Where t, is thickness of the die, K is thermal conductivity and A is cross-section area of the die. Thickness and thermal conductivity of the dies are the same as the dies from the same wafer batch. The cross-section area size of the dies is also the same. Hence, its influences are negligible.

In-line thermal transient testing

The most accurate method to detect gaps (e.g. cracks) between die junction and package substrate is by measuring the thermal resistance. This method is more sensitive than measuring the increases of electrical resistance. However, standard thermal resistance measurement needs special equipment and long testing time for measurement of the V_f temperature coefficient to correlate the V_f of the LED to the Junction Temperature. This is not practical for in-line testing, as long test time will reduce productivity in mass manufacturing environment. However, this detection method can be adapted to with some modification.

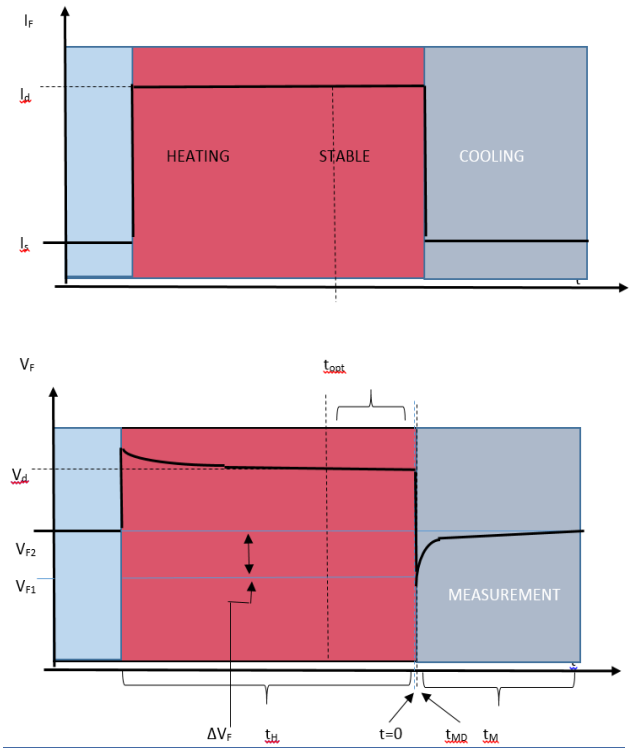
Similar to a standard thermal resistance measurement, the new testing method (ΔV_f sequence test) measures the voltage different between the device in a hot state during drive current and a cool state at low current. This measurement method follows a simple test sequence on the production tester as illustrated in Figure 11. After binning tests, devices with a crack have a higher junction temperature, due to a higher thermal resistance; hence V_{f1} is lower compared to a die without cracks. During the cooling phase the dies with or without crack cool down close to the room temperature. The V_{f2} is nearly independent whether the die is with or without crack. The ΔV_f is higher for die with crack because of the lower V_{f1}. V_{f1} is low for crack die because the die still hot due to high R_{th}.

The inline thermal transient testing or ΔV_f sequence test requires a very high speed measurement with hardware capabilities responding to test the samples at measurement speeds in micro-seconds and micro-volts. A built-in hardware is vital, to reduce stray capacitance and noises that could impact the repeatability and reproducibility of the measurements. The thermal transient of the LED must be captured within one millisecond. If not, the thermal transient will be lost. Hence, the measurement will not be accurate. The switching from driving current, I_d to sensing current I_s must be quick within 5 microseconds. The sensing, data acquisition and processing have to be quick within several milliseconds. The whole inline thermal transient testing has to be within several milliseconds to match the existing inline testing speed. If it has been too long, the productivities will be affected. Hence, it will no longer be economical to for inline testing.

In this experiment we can demonstrate the new apparatus using TSP method to isolate units with and without cracks effectively and it able to match the inline testing speed. A total of 300 units (that were bonded with 60 gF, 100 gF and 140 gF) were tested. The result was very encouraging as the entire cracked die units (with bond force 100 gF and 140 gF) were tested out as rejects. All the units without cracks (60 gF cell) units passed. We repeated the test and confirmed the same result. All die cracked units failed the test. This ΔV_f Test sequence is successfully able to detect these cracked units. It confirms the effectiveness of this measurement technique.

Conclusion

This investigation indicates that R_{th} of AlInGaP die increases as the crack severity increases because of an increase in the bond force. This is due to the thermal path of the die is impeded by the gap caused by the cracks. The larger cracks introduced higher R_{th} values. This research work also revealed an interesting finding, that the method employed for mesuring the R_{th} of the crack die with fast switching TSP method can be deployed for inline testing to separate dies with and without crack as the temperature rise in short time-scales at junction sufficient for seclusion of units with cracks and without cracks. This was confirmed



V_{f2} is voltage of cool device biased by sensing current

V_{f1} is voltage of hot device biased by sensing current

~5 µs <t_M< 1 ms

The measurement time t_M has to be between 5 µs to less than 1 ms, in order to capture the thermal transient of the LED.

Figure 11: Illustrating the forward current and voltage during the thermal testing (JEDEC).

in this research work by the ΔV_f sequence test. However, this test has to be confirmed with large scale samples as current research is limited to only several hundred units .

Acknowledgements

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