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The Push to Continue the Progression of Moore's Law

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Despite continued apprehension in face of the difficulties of continuing to increase the power and performance of integrated circuits (ICs), the current view is that optical lithography will continue to progress down to 1 nm critical dimension (CD). Moore's law, which states that the density of transistors in an integrated circuit will double every 1-2 years, has been good for 45 years and is set to continue for the next 8-10 years. The relative immaturity of nanoimprint lithography and the low throughput of electron beam lithography systems mean that optical lithography is set to shoulder the burden of carrying Moore's law to higher density circuits. At present, the Argon fluoride laser, with a wavelength of 193 nm, allows a CD of 38 nm which is reduced to 19 nm by double patterning and to 10 nm using quadruple patterning. Future generations of optical lithography system will be based on EUV laser, with a wavelength of 13.5 nm, which will drive the CD to 7 nm, followed by 4 nm, and then 1 nm. The EUV laser is generated from a plasma produced by the irradiation of tin drops by a high power carbon dioxide laser.

In order to take transistor devices to the new sub-10 nm nodes, replacement gate processes have been used in conjunction with silicon nanowires to develop gate-all-round transistors. The horizontal alignment of the nanowire allows vertical stacking of transistors. An alternative to the silicon nanowire is the carbon nanotube which holds promise for sub-nanometre channel lengths. Atomic layer deposition and etching techniques are being developed for sub-nanometre layer thickness control. Spintronics is used in hard drives and magnetic random access memories for data which is encoded in single spin-encoded electrons. It is one technology which holds solving the high density memory requirement of future ICs.

One of the drivers of the $350-billion-dollar IC industry is the Internet of Things, a futuristic view of the world where a variety of consumer products have their own IC and associated components which can communicate with other devices and systems. Low power ICs are key to the future success of this project. Ultra-low power nodes reduce supply voltages and utilize SRAMs optimized for low leakage currents. Automotive and sensor, in particular biometric, gas, and image, products are more defined alternative future applications for ICs. The next-generation mobile handset will employ chip stacking based on an integrated fan-out process (InFO), for integrating DRAM with cost-sensitive ICs. InFO comes in two versions. One links a logic chip to DRAM memory; another version can stack multiple chips on top of another without a silicon interposer.

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