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Analytical Vth, DIBL and Swing with and without Effective Conducting Path Effect (ECPE) for the Submicronic SDG FD SOI MOSFET

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Abstract

We are presenting a convergence study of the evanescent model and the polynomial model with and without the Effective Conduction Path Effect (ECPE). These analytic models of the electric potential in the channel are used to analyze the short channel effect for the submicronic Symmetric DG FD SOI MOSFET. In this paper, we figure out the 2D Poisson equation and we analytically write using the evanescent model, the surface potential, the threshold voltage, the DIBL and the sub-threshold swing. The natural scale length for the polynomial model λ_p and its corrected form λ_{pc} including the ECPE are mentioned. The results, of the analysis of the short-channel effects (SCEs), show a good agreement of the evanescent model and the polynomial model including the ECPE with measures done by simulation tools.

Keywords: Evanescent and polynomial models; Effective conduction path effect; Surface potential; Threshold voltage; DIBL; Sub-threshold swing; Symmetric double gate fully depleted SOI MOSFET

Introduction

The electronic industrial world is in continuous search for an amelioration of the speed and the consumed power of the MOSFET device. But, with the miniaturization of the shape, governed by the ITRS roadmap [1], this component has shown its defects due to the parasitic effects. Among these undesirable effects, the so called short channel effects (SCEs), which minimize the MOSFET performances [2] and perturb the IC function.

The microelectronic industrials have sought to avoid these defects. The MOSFET structure on silicon with multiple gates [3-6] has proved successful in increasing the duration of the miniaturization and improving the compound performances taking into consideration the preservation of the planar silicon technology.

Despite its complex technological realization, the Symmetric DG FD SOI MOSFET remains one of the most interesting and encouraging compound to realize the Ultra-Deep Sub-Micronic (UDSM) structure and throughout augment density of integration.

Many models [7-13] have been developed to examine the performance of components. In this paper, we will put the evanescent model and the polynomial model with and without the ECPE into consideration to find out their convergence points for the study of the SDG FD SOI MOSFET. We solve the 2D poisson equation and we, analytically, analyze the SCEs via the dispersion study of the surface potential and the threshold voltage along the channel as well as the DIBL effect and the sub-threshold swing. The natural scale length for the polynomial model λ_p and its corrected form λ_{pc} including the ECPE are mentioned. The analysis of the SCEs allows us to locate the convergence points of the utilized models. We confirm these convergence situations by simulator data and/or some measures.

Evanescent Model

Surface potential and threshold voltage

Figure 1 illustrates the cross section of the symmetrical DG SOI MOSFET device under fully depleted conditions and the inversion charge is neglected in regard to that of the of the depletion. We define by L, distance between source and drain, the channel length. t_{ox} and t_{si} represent respectively the thickness of the frontal oxide and the silicon body thickness. N_a is the silicon doping in the channel and N_d is the doping concentration of the source and drain regions. ε_{si} and ε_{ox} represent respectively the dielectric permittivity of the silicon film and the silicon dioxide.

The evanescent model supposes that the electrostatic potential in the silicon film, overlapped between both grids, is represented, according to the superposition principle, by $\varphi(x,y) = \varphi_1(x) + \varphi_2(x,y)$. $\varphi_1(x)$ is the solution of Poisson equation for a long channel and $\varphi_2(x,y)$ is the solution of the Laplace equation and contain the short channel effect [14].

$$\frac{d^2\varphi(x,y)}{dx^2} + \frac{d^2\varphi(x,y)}{dy^2} = \frac{qN_a}{\varepsilon_{si}} \quad (1)$$

The necessary boundary conditions of φ_1 and φ_2 to define $\varphi(x)$ are as follow:

For φ_1:

$$\varphi_1\left[\frac{\pm t_{si}}{2}\right] = V_{SL} = \varphi_{gf} \cdot \frac{qN_a t_{si}}{2C_{ox}}$$

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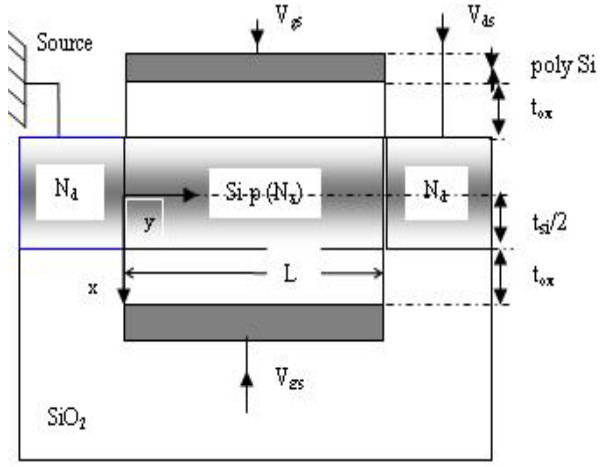

Figure 1: Schematic cross section of a symmetric DG FD SOI MOSFET device.

$$\left[\frac{\partial\varphi_1}{\partial x}\right]_{x=\pm t_{si}/2} = \frac{Cox}{\varepsilon_{si}}.\left(\varphi_1\left[\frac{\pm t_{si}}{2}\right] - \varphi_{gf}\right)$$

$$\left[\frac{\partial\varphi}{\partial x}\right]_{x=0} = 0,$$

Where $\varphi_{gf} = V_{gf} - V_{fb}$, V_{SL} represents the surface potential for a long channel at $= \frac{\pm t_{si}}{2}$; V_{fb} is the flat band voltage at the interface grid oxide – poly-silicon substrate.

$C_{ox} = [\varepsilon_{ox}/t_{ox}]$ is the frontal oxide capacitance and Csi = $[\varepsilon_{si}/t_{si}]$ is the silicon body capacitance.

For φ_2:

$$\varphi_2(x, y=0) = V_{bi} - \varphi_1(x)$$

$$\varphi_2(x, y=L) = V_{bi} + V_{ds} - \varphi_1(x)$$

$$\partial\varphi_2 / \partial x)_{x=\pm t_{si}/2} = C_{ox} / \in_{si} .\varphi_2(x = \pm t_{si}/2, y)$$

$$\partial\varphi_2 / \partial x)_{x=0} = 0$$

Where $V_{bi} = [KT / q.Ln(N_a N_d / n_i^2)]$ denotes the built-in voltage between the source/drain end.

The frontal surface potential is defined as:

$$\varphi_{sf}(y) = \varphi_1(x = \pm t_{si}/2) + \varphi_2(x = \pm t_{si}/2, y)$$

and written as follow:

$$\varphi_{sf}(y) = V_{SL} + (V_{bi} + V_{ds} - V_{SL})\frac{\sinh(y/\lambda_e)}{\sinh(L/\lambda_e)} + (V_{bi} - V_{SL})\frac{\sinh(L - y/\lambda_e)}{\sinh(L/\lambda_e)} \quad (2)$$

Where λ_e represents the characteristic length for the evanescent model and verify the follow equality:

$$\sin(t_{si}/2\lambda_e) - \lambda_e.\cos(t_{si}/2\lambda_e).C_{ox}/\in_{si} = 0 \quad (3)$$

The threshold voltage is defined as a grid voltage (V_{gf}=V_{th}) for φ_{sf}=2$\emptyset_B$ at y=y_0 where $\phi_B = [KT / q.Ln(N_a / n_i)]$ is the Fermi potential in the channel and y_0 is the minimum surface potential abscise. This leads to write V_{th} as the form:

$$V_{th} - V_{fb} = \frac{q.N_a.t_{si}}{2C_{ox}} + \{2\phi_B - (V_{bi} + V_{ds}).\sinh(y_0/\lambda_e)/ \sinh(L/\lambda_e) - V_{bi}\sinh(L - y_0/\lambda_e)/\sinh(L/\lambda_e)\}.\gamma_s^{-1} \quad (4)$$

Where γ_s denotes the short channel effects [15] and written as:

$$\gamma_s = (1 - \sinh(y_0/\lambda_e)/\sinh(L/\lambda_e) - \sinh(L - y_0/\lambda)/\sinh(L/\lambda_e))$$

The gradient of threshold voltage is defined as $\Delta V_{th} = V_{th0} - V_{th}$ where V_{th0} denotes the threshold voltage for a long channel SDG FD SOI MOSFET and written as:

$$V_{tho} = 2\phi_B + \frac{q.N_a.t_{si}}{2C_{ox}} + V_{fb} \quad (5)$$

DIBL parameter

For the SDG FD SOI MOSFET with short channel, the surface potential minimum increase with the drain bias. Thus, the short channel effect is attributed to the penetration of the electric field line, of the drain-channel junction, in the channel resulting in the potential barrier lowering (DIBL effect). This leads to the decreasing of the threshold voltage.

The $\Re$ parameter defined by $\Re = \partial V_{th}/\partial V_{ds}$ evaluates the DIBL effect and written as:

$$\Re = \{\sinh(y/\lambda_e)/\sinh(L/\lambda_e)\}.\gamma_S^{-1} \quad (6)$$

Sub-threshold swing

The sub-threshold slope, appealed swing, is defined as the grid voltage that modifies the drain current under a threshold of a decade and written as

$$S = \frac{KT}{q}.Ln_{(10)}.\gamma_s^{-1}(y = y_0) \quad (7)$$

Where y_0 is the minimum surface potential abscise.

Polynomial Model

Without the ECPE

Taking into account the polynomial model which considers the conduction current is at the surface of the silicon body and supposes parabolically the electrostatic potential profile in the vertical direction [6,10].

$$\varphi(x, y) = C_0(y) + C_1(y).x + C_2(y).x^2 \quad (8)$$

Using the classical boundary conditions:

$$\varphi(x = \pm t_{si}/2, y) = \phi_{sf}(x)$$

$$\varphi(x = 0, y) = \phi_c(y)$$

$$\partial\varphi(x, y)/\partial x|_{x=\pm t_{si}/2} = C_{ox}/\varepsilon_{si}.(\varphi_{sf}(y) - \varphi_{gs}$$

$$\partial\varphi(x, y)/\partial x|_{x=0} = 0$$

and writing the Poisson equation as $\varphi_{sf}(x = \pm t_{si}/2, y)$, we deduce the polynomial characteristic length

$$\lambda_p = (\varepsilon_{si}.t_{si}/2C_{ox})^{1/2} \quad (9)$$

Including the ECPE

The notion of the ECPE supposes that the gravity centre of the conduction current is at $x=d_{eff}$. The presentation of the electrostatic potential $\varphi(x, y)$ at $x=d_{eff}$ allows us to bring about a correction to polynomial characteristic length λ_p.

The new corrected characteristic length corresponding to the polynomial model including ECPE is:

$$\lambda_{pc} = \lambda_p (1 + \frac{C_{ox}}{\varepsilon_{si}} . d_{eff} - \frac{C_{ox}}{\varepsilon_{si} t_{si}} . d_{eff}^2)^{1/2} \quad (10)$$

The key factor d_{eff}, which illustrates the variation of scaling nature length λ_{pc} with substrate doping density, is so-called depth of the effective conducting path and it presents the location where the punch-through current mainly occurs at subthreshold conduction with ECPE conducting mode [10].

The evanescent model and the polynomial model with and without the ECPE are utilized to analysis the short channel effect with the intention of searching the situations of their convergence.

Results and Discussion

To verify the analytical models of the convergence of SCE's, the graphs illustrating le surface potential, the threshold voltage, DIBL and swing were plotted, compared and verified by measurement data. The same work for the conventional MOSFET prove that the convergence situation for the evanescent model and the polynomial model including ECPE is at $d_{eff}=0.5t_{si}$ [16] and at $d_{eff}=0.35t_{si}$ [17] for the single-gate SOI MOSFET device.

For the three models, figure 2 shows the evolution of the characteristic length λi *(i=e, p or/and pc)* as a function of ratio (t_{ox}/t_{si}) for $N_a=4.10^{17}cm^{-3}$, $V_{ds}=0.5V$ and for a large range of t_{si} (t_{si}=1,5 and 10nm). We notice an adequate convergence, at $d_{eff}=0.25t_{si}$, between the evanescent model and the polynomial model including the ECPE. We also see that this convergence situation coincide with the data of equation 27 cited by Chen [13].

Figure 3 presents the evolution of the surface potential minimum and its position along the channel for the submicronic SDG FD SOI MOSFET device and for V_{ds}=0.5 and 2.5V. The results, and on a large scale of drain bias, show a good agreement between the evanescent model and the polynomial model including the ECPE at $d_{eff}=0.25t_{si}$.

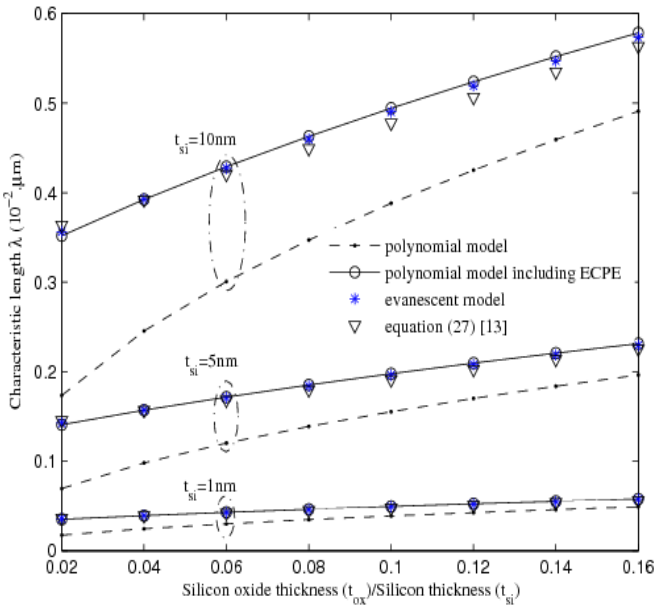

Figure 2: Characteristic length λ_i versus ratio (t_{ox}/t_{si}).

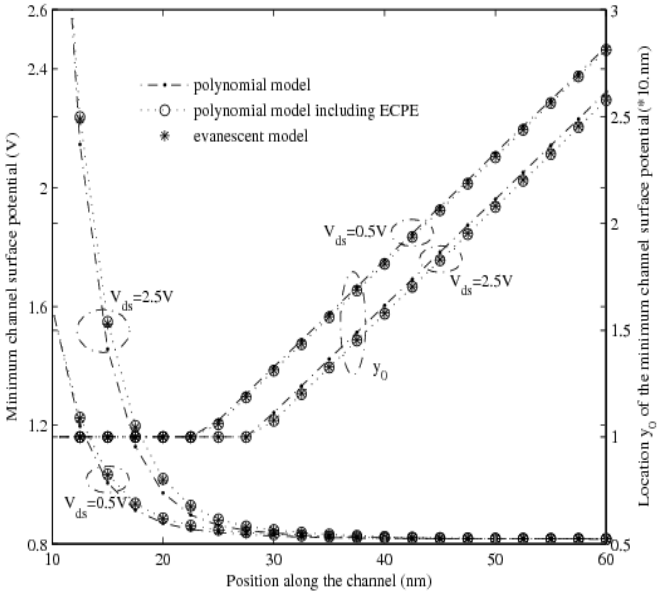

Figure 3: Minimum channel surface potential and its location y0 as a function of position along the channel for different values of drain bias.

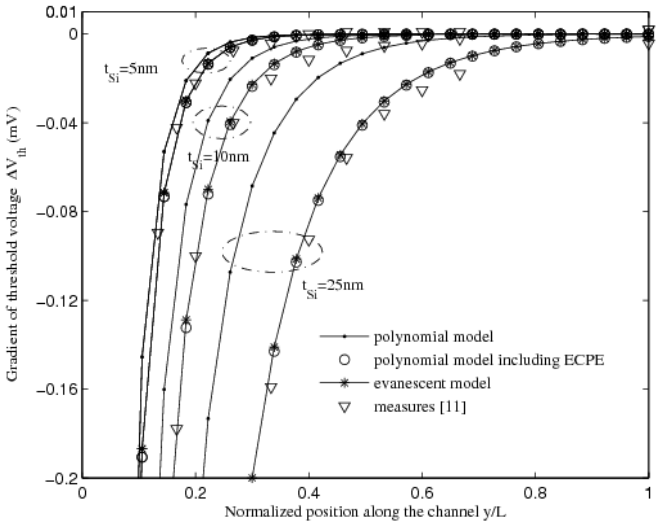

Figure 4: Variation of threshold voltage gradient versus normalized position along the channel y/L.

Figure 4 illustrates the evolution of the threshold voltage gradient in regard to the normalized position to L along the channel for L=150nm, V_{ds}=1.5V, t_{ox}=1.5nm and for t_{si}=5, 10 and 25nm. These results prove a perfect agreement, at $d_{eff}=0.25t_{si}$, between the evanescent model and the polynomial model including the ECPE with Jaju's measurements [11].

As the drain voltage increases, the channel barrier and the threshold voltage are reduced. This is called Drain Induced

Barrier lowering. Figure 5 shows the evolution of the DIBL parameter as function of normalized position along the channel for the ultra-thin SDG FD SOI MOSFET with L=150nm, V_{ds}=1.5V, t_{ox}=1.5nm and for t_{si}=5 and 10nm. Measures data [11] agree closely with the

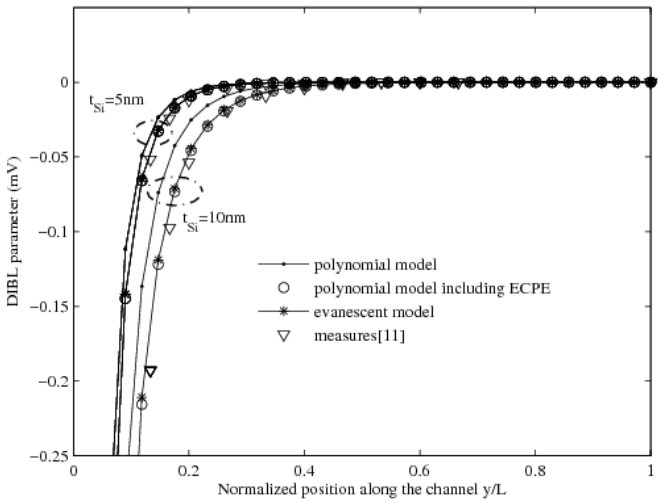

Figure 5: DIBL parameter versus normalized position along the channel y/L.

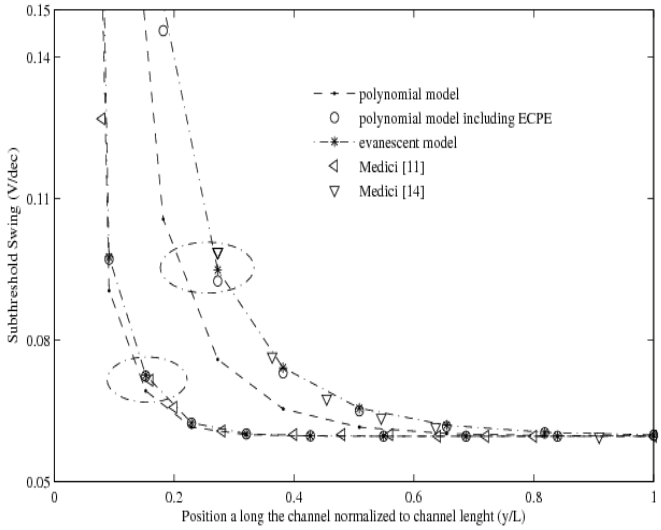

Figure 6: Variation of the Sub-threshold Swing with normalized position along the channel y/L.

predictions of the evanescent model and the polynomial model including the ECPE at $d_{eff}=0.25t_{si}$.

Figure 6 presents the sub-threshold swing parameter, in weak inversion, as a function of normalized position a channel length for t_{ox}=1.5nm, t_{si}=10nm, $N_a=1.10^{17}cm^{-3}$ and V_{ds}=1V [11] and for t_{ox}=1.5nm, t_{si}=20nm, $N_a=1.10^{16}cm^{-3}$ and V_{ds}=1V [18]. We notice an adequate convergence, at $d_{eff}=0.25t_{si}$, between the evanescent model and the polynomial model including the ECPE with Jaju's measurements [11] as well as those of MEDICI's [14].

Conclusion

The study of the short channel effects through the surface potential, the threshold voltage, the DIBL and the sub-threshold swing has proved the convergence situation of the evanescent model and the polynomial model including the ECPE. The convergence situation for the ultra-thin SDG FD SOI MOSFET's device is at $d_{eff}=0.25t_{si}$.

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