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The Heart of an Embedded Systems Engineer

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No one can deny the thrill of creating magnificent desktop, web or mobile applications using high-level programming languages. No one can deny the need to move towards higher levels of abstraction in order to design more vast and complex software systems. But what happens when you need massive number crunching, or soft/hard real–time applications that deal with crucial needs, such as processing images on the fly from a push broom scanner in space and sending them directly to Earth. It is very convenient to implement an application, never having to worry about memory limitations, but what happens when you are implementing a signal analysis engine for an accelerometer having a microcontroller running an RTOS and various applications, and its memory being able to handle no more than 128 samples for an FFT calculation within one measurement in real-time? Most of the software enthusiasts will go with the OOP capabilities and ease of high-level languages and would not bother with memory handling, performance, throughput, timing constraints the way an embedded (Software/FPGA) engineer would.

As an embedded software engineer who has also written VHDL code implementing complex signal/image processing algorithms on FPGAs, I have come to the conclusion that there is nothing more intriguing than dealing with bit-level manipulation, number representations (floating-point and fixed-point approximation), parallel programming aspects, clocks and timing and having the architecture/hardware picture before your eyes, like Neo with the *Matrix* code, the HW/SW interface within your grasp. Having the ability to understand the machine and thoroughly command it.

On the one hand there is the joy and challenge of designing a complex data-path and its control at the RTL level with VHDL/Verilog and there you go; a new image compressor, utilizing a Discrete Wavelet Transform and a Bit-Plane Entropy Encoder. Especially, when it comes to DSP, the sky is the limit with the massive parallelism of an FPGA or the multi-core arena of a GPU. On one hand there is VLSI (FPGA) design of a core, a chip. On the other hand, there is the embedded system, a collection of chips. A combination of microcontrollers and DSPs, memory, bus protocols, interfaces and hardware accelerators, all governed by the beautiful C programming language, or even ASSEMBLY in some cases.

Since I have worked with DSP applications, the design time for FPGA product can be too long and time-to-market pushes you not to test alternative algorithm architectures. That is a drawback. However, we live in great times and technology advancement has brought us the all-programmable System-On-Chip (SoC). Software and hardware programmable and all through one seamless design flow using one language, such as–wait for it–C (C-like anyway)! Either with Xilinx's HLS or Altera's OpenCL SDK, one can experiment with different algorithms, architectures and all sorts of tweaks and tricks in a flash and implement them writing C code for both the software and hardware components. Especially with OpenCL code, can utilize all aspects of parallelism and run on CPUs, GPUs, DSPs or FPGAs! High-level abstraction has done it again, only this time the embedded engineer can do it all. Complete and utter programmability. Software and hardware acceleration, tightly coupled. What are the limits now?

I can imagine embedded systems (and the power of SoCs) exploring the very darkness of the universe, enhancing every device, automobile and network, aiding other sciences and experiments, sensing all kinds of physical phenomena, controlling all home appliances and even saving lives.

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